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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/066,061

01/30/2002

Spiros Kalogeropoulos

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7590

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EXAMINER

STEELMAN, MARY J

ART UNIT

PAPER NUMBER

2122

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/066,061

Applicant(s)

KALOGEROPULOS, SPIROS

Examiner

Mary J. Steelman

Art Unit

2122

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 1/30/2002, 5/10/2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 May 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/10/2002</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claims 1-29 are pending.

#### ***Information Disclosure Statement***

2. IDS received 10 May 2002 has been considered.

#### ***Drawings***

3. Drawings received 25 April 2002 must have "REPLACEMENT SHEET" noted at the top margin. **INFORMATION ON HOW TO EFFECT DRAWING CHANGES**

#### **Replacement Drawing Sheets**

Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment. Any replacement drawing sheet must be identified in the top margin as "Replacement Sheet" (37 CFR 1.121(d)) and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin.

#### **Timing of Corrections**

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.85(a). Failure to take corrective action within the set period will result in ABANDONMENT of the application.

If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may **NOT** be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability.

#### ***Claim Rejections - 35 USC § 103***

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,367,651 to Smith et al.

Per claims 1, 28 and 29:

Smith disclosed:

-method...system...computer program product...

(Smith: Col. 2, lines 16, "method and apparatus (system)...", col. 2, lines 20-2, "has particular application to code (computer program product) compilers of compilers for target machine that support parallel instruction execution..." It is inherent that a system encodes on a computer program product to perform the invention.)

-allocating registers;

(Smith: Col. 2, lines 35-37, "Upon invocation, the improved register allocator determines and prioritizes regions...", col. 2, lines 43-44, "Then, the improved register allocator allocates registers...")

-building a trace comprising basic blocks;

(Smith: Col. 5, lines 28-29, "...the translator builds loop table, orders instruction blocks (basic blocks), constructs data flow graphs etc...")

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-scheduling instructions within said trace after said allocating registers

(Smith: Col. 2, lines 45-50, "After allocating registers for each region...tie improved instruction scheduler...then invoked...schedule the instructions...")

Smith failed to specifically disclose "building a trace comprising basic blocks". However, he did disclose a translator that provides compiler information, including basic blocks. And the basic blocks are divided into regions, which are optimized individually (col. 2, lines 35-37).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, that a region optimization, as disclosed by Smith would require a 'trace' of region unoptimized code, after which the features of Smith's invention, allows each trace / region to be optimized prior to being merged into a complete program.

Per claims 2 and 20:

- scheduling instructions comprises moving instructions between said basic blocks.

(Smith: Col. 3, lines 3-11, "...register allocator invokes the instruction combiner to replace combinations of instructions with equivalent single combined instructions that are not being executed in parallel...invokes the improved instruction scheduler...to update the preliminary instruction schedule if the instruction combiner altered the instructions to be generated...", lines 23-26, "the improved instruction scheduler provides the improved loop unroller with a preliminary instruction schedule that indicates the amount of parallelism that can be achieved.")

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Per claims 3 and 21:

-building a control flow graph comprising said basic blocks.

(Smith: col. 5, lines 28-30, “translator builds loop table, orders instruction blocks (control flow graph), constructs data flow graphs, etc....”)

Per claims 4 and 22:

-control flow graph comprises an off trace basic block.

(Smith: Smith disclosed a register allocator that (col. 7, lines 15-16, “determines and prioritizes the regions of a program...” Each region is a collection of basic blocks (col. 7, lines 21-22).

Smith disclosed successor and predecessor basic blocks (col. 7, lines 20-40). An off trace block may be the preceding or succeeding regions, that will subsequently be optimized. Col. 7, lines 16-17, “The program is divided into regions to localize the optimizations.”)

Per claims 5 and 23:

-scheduling instructions comprises recognizing data dependencies from said off trace basic block.

(Smith: Code is partitioned into regions to localize optimizations (col. 7, lines 16-17). Col. 7, lines 12-16, “...upon receiving the intermediate representations and their associated information (data dependencies) from the translator as inputs...”, col. 7, lines 21-24, “A region comprises a collection of basic blocks which satisfy the following predecessor and successor relationship rules (dependencies) with basic blocks outside the region...” The scheduler is called by the translator and will recognize the off trace basic blocks.)

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Per claims 6, 17, and 24:

-scheduling instructions comprises computing height information of said instructions.

(Smith: Col. 7, lines 41-55, "...selects an unallocated region with the highest priority...and prioritizes the register candidates...determined based on use and definition counts of the register candidates in the region...invokes the improved scheduler..." The allocator computes height information then invokes the scheduler.)

Per claims 7, 18, and 25:

-height information is computed using execution probabilities of said basic blocks.

(Smith: Col. 7, lines 41-55, "...selects an unallocated region with the highest priority...and prioritizes the register candidates...determined based on use and definition counts of the register candidates in the region...invokes the improved scheduler..." The allocator computes based on use and definition counts (execution probabilities).)

Per claims 8 and 26:

-said height information is computed using adjusted execution times of said instructions.

(Smith: Col. 7, lines 41-55, "...selects an unallocated region with the highest priority...and prioritizes the register candidates...determined based on use and definition counts of the register candidates in the region...invokes the improved scheduler...")

Per claims 9 and 27:

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- scheduling instructions comprises computing an adjusted execution time of an instruction of said instructions by multiplying an execution time of said instruction by an execution probability factor.

(Smith: Col. 7, lines 41-55, "...selects an unallocated region with the highest priority...and prioritizes the register candidates...determined based on use and definition counts of the register candidates in the region...invokes the improved scheduler...")

Per claim 10:

- scheduling instructions comprises generating compensation code.

(Smith: Smith recognizes that register allocation may require 'spill code' to be generated. Col. 9, line 67-col. 10, line 1, "...spill code (generating compensation code) will have to be introduced.")

Per claim 11:

- scheduling instructions comprises:

-building a trace block comprising said instructions;

(Smith, col. 7, lines 12-17, "...upon receiving the intermediate representations and their associated information from the translator as inputs, the improved register allocator determines and prioritizes the regions of a program...The program is divided into regions to localize the optimizations." A region (trace block of instructions) is optimized.)

-scheduling said instructions within said trace block;



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(Smith: Col. 7, lines 54-58, "...the improved register allocator invokes the improved scheduler...provides...a preliminary schedule...")

-moving said instructions from said trace block to said basic blocks.

(Smith: Col. 8, lines 39-40, "The process...is repeated for each region...", col. 6, lines 40-44, "When invoked in 'final mode', the improved scheduler receives the unrolled intermediate representations and associated information as inputs. In response, it determines the final instruction schedule (each region / trace block is merged into a complete program of basic blocks and final instructions are scheduled)...")

Per claim 12:

A method comprising:

- allocating registers;
- building a trace after said allocating registers,
  - said trace comprising basic blocks comprising instructions;
- building a trace block comprising said instructions;
- scheduling said instructions within said trace block;
- moving said instructions from said trace block to said basic blocks.

(See limitations addressed in claims 1 and 11 above.)

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Smith failed to specifically disclose “building a trace comprising basic blocks’. However, he did disclose a translator that provides compiler information, including basic blocks. And the basic blocks are divided into regions, which are optimized individually (col. 2, lines 35-37).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, that a region optimization, as disclosed by Smith would require a ‘trace’ of region unoptimized code, after which the features of Smith’s invention, allows each trace / region to be optimized prior to being merged into a complete program.

Per claim 13:

- said building a trace block comprises inserting a join instruction into said trace block, said join instruction being a delimiter for a first basic block of said basic blocks.

(Smith: Smith discloses a trace block (region) that is individually optimized (localize the optimizations, col. 7, line 17), and repeated for each region (col. 8, line 39). Regions are joined into a complete program. Col. 8, lines 43-45, “The global register allocation for the various regions are then merged together...” Merged code is reconciled (col. 8, line 48).)

Smith does not specify a ‘join instruction’, but does specify that the optimized code for each region is merged and reconciled, and thus a type of ‘join instruction’ would be obvious.

Per claim 14:

- updating a use set of said join instruction with a global live-in for an off trace basic block.

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(Smith: Col. 8, lines 43-45, “The global register allocation for the various regions are then merged together...” Merged code is reconciled (updating a use set of said join instruction) (col. 8, line 48).)

Smith does not specify a ‘join instruction’, but does specify that the optimized code for each region is merged and reconciled, and thus a type of ‘join instruction’ would be obvious.

Per claim 15:

- said global live-in is a set of registers which contain live values when entering said off trace basic block.

(Smith: Smith disclosed consideration of register sets of the program as a whole (when entering said off trace basic block) Col. 8, lines 43-48, disclose that the global register allocation for the various regions are merged. Col. 9, lines 9-41, Smith disclosed consideration given to a “register candidate that is live through multiple blocks” and techniques to allocate registers.)

Per claim 16:

- an instruction of said instructions which defines a value in said set of registers is not moved past said join instruction during said scheduling said instructions.

(Smith disclosed some instructions are not moved. Col. 8, lines 24-34, “Then the improved register allocator determines the optimal partition for global and local registers...determines the optimal partition by determining whether the improved register allocator or the improved scheduler can better utilize a particular register (instruction in not moved past said join

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instruction during scheduling, depending on best utilization)...the improved register allocator determines the utility based on usage and definition counts. It will be appreciated that the improved register allocator may be implemented with a variety of other utility determination functions.”)

Smith did not explicitly disclose ‘an instruction of said instructions which defines a value in said set of registers is not moved past said join instruction during said scheduling said instructions’, but rather broadly disclosed that the best utilization of registers will be chosen and it may be determined based on usage and definition counts. Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Smith to include details such as ‘an instruction of said instructions which defines a value in said set of registers is not moved past said join instruction during said scheduling said instructions’ because he disclose that a variety of utility determination functions may be used in the determination.

Per claim 19:

A system comprising:

-processor;

(Smith: col. 4, line 19, “...CPU...”)

-a memory having a method of scheduling instructions therein, wherein upon execution of said method, said method comprises:

(Smith: Col. 4, line 19, “...memory...”)

-allocating registers;

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(Col. 5, lines 34-43, “The improved register allocator...allocates the global registers...”)

-building a trace comprising basic blocks;

(Smith: Col. 7, lines 12-16, “...upon receiving the intermediate representations and their associated information (basic blocks) from the translator as inputs...register allocator determines and prioritized the regions of a program (a trace of basic blocks).”

-scheduling instructions within said trace after said allocating registers.

(Smith: Col. 7, lines 52-58, “...register allocator ...invokes the improved scheduler...provides the improved register allocator with a preliminary schedule...” Within the selected region (basic block trace) instructions are scheduled.)

Smith failed to specifically disclose “building a trace comprising basic blocks’. However, he did disclose a translator that provides compiler information, including basic blocks. And the basic blocks are divided into regions, which are optimized individually (col. 2, lines 35-37).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, that a region optimization, as disclosed by Smith would require a ‘trace’ of region unoptimized code, after which the features of Smith’s invention, allows each trace / region to be optimized prior to being merged into a complete program.

Also, see limitations addressed in claims 1 & 11 above.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant’s disclosure.

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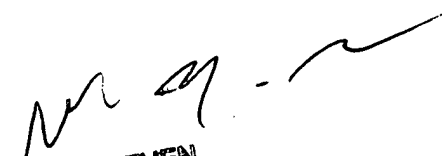
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman



01/06/2005

  
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PRIMARY EXAMINER